L.6: Resistive memory switching in ultra-thin films of TiO_2

Resistive switching memories have recently shown tremendous potential to overcome the physical and technological limitations of existing CMOS based memory technology. The resistive switching devices store information through transition between two states of resistances (low and high) on application of bias voltage. We, at Laser Material Processing Division of RRCAT, recently observed electric field controlled reproducible non-volatile unipolar resistive memory switching in amorphous ultrathin TiO_2 films of thickness ~ 4 nm in Au/TiO_2/Pt device configuration. For these studies the ultrathin amorphous layers of TiO_2 were grown by optimized thermal atomic layer deposition on Pt/TiO_2/SiO_2/Si (100) substrates and top electrodes of Au of diameter ~ 200 μm and thickness ~ 50 nm were deposited by DC sputtering using shadow masking. The schematic of two terminal resistive memory cells is shown in inset of Fig. L.6.1. The current-voltage (I-V) measurements of the Au/TiO_2/Pt devices were carried out using a source and measuring unit (Keithley-2611 A) at room temperature in top-bottom geometry.

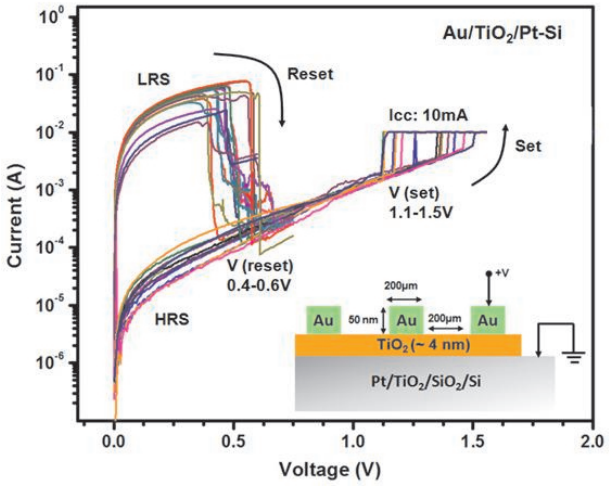

Fig. L.6.1: Current-Voltage characteristics of Au/TiO_2/Pt devices at current compliance of 10 mA showing resistance switching between low and high resistance states (LRS and HRS) for 50 test cycles. Inset shows schematic of memory devices.

All the as grown devices exhibited initial low resistance state (LRS) with resistance of ~ 5 Ω. Due to extreme thinness and amorphous nature of TiO_2 layer, these devices did not require electro-forming process to initiate resistive switching cycles which is highly beneficial for practical applications as the negative effect of electroforming process such as destruction of electrode is avoided. The I-V characteristics of Au/TiO_2/Pt devices are shown in Fig. L.6.1 where a clear switching of the resistance of the device on voltage sweep at fixed compliance current can be easily witnessed. The device in the high resistance state (HRS) showed resistance of ~ 12 kΩ. The resistance states (lowor high) thus obtained remained unaltered even in absence of applied voltage confirming non-volatility.

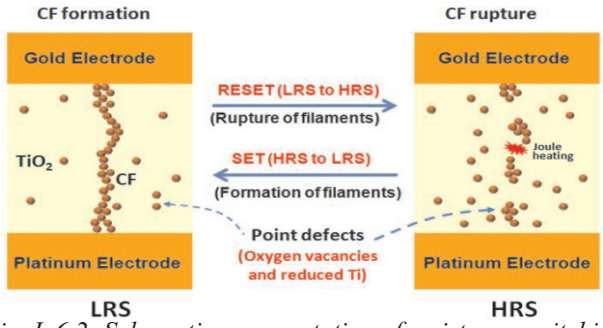

Fig. L.6.2: Schematic representation of resistance switching mechanism by formation and rupture of conducting filaments in TiO_2 matrix on voltage sweep with current compliance.

A large resistance ratio of ~ 10^3 between high and low resistance states along with excellent data retention and endurance characteristics were observed, which are pre-requisites for practical memory applications. The switching voltages (V_{set} and V_{reset}) were preferably below 1.5 V as shown in Fig. L.6.1 with a clear operating window between them. The observed sharp set (switching from HRS to LRS) and gradual reset (switching from LRS to HRS) processes clearly indicated the formation and rupture of nano-sized conducting filaments (CFs) consisting of point defects such as oxygen vacancies and reduced Ti, as dominant switching mechanism which was further corroborated by temperature dependent I-V measurements of the devices. Presence of these point defects in as grown TiO_2 films was confirmed by X-ray photoelectron spectroscopy. The formation of CFs through agglomeration of point defects due to applied electric field during set process and their rupture due to Joule heating during reset process bringing low and high resistance states respectively is schematically shown in Fig. L.6.2. Preliminary investigations on switching speed of these devices indicated that the set process is much faster (~1000 times) than the reset process. Further investigations on the switching speed of the devices and its correlation with compliance current are currently in progress. Our initial findings clearly show that ultra thin amorphous TiO_2 is a promising material for next generation low power, high speed, and ultra-dense nonvolatile resistive memory switching devices for information technology. For more details, please refer to *V.K. Sahu et al., Proc. 60th DAE Solid State Physics Symposium, Amity University, Noida, Dec. 21-25, 2015.*

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